M-MOS Semiconductor Hong Kong Limited

38V P-Channel Enhancement-Mode MOSFET

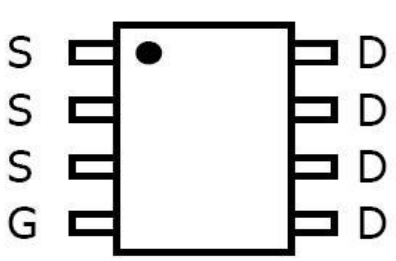
V_{DS}= -38V

$R_{DS(ON)}$, V_{gs}@-10V, I_{ds}@-14A = 15mΩ

Features

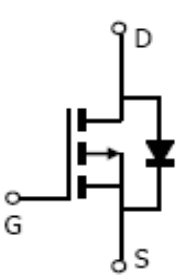
Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance

SO-8



Top View

Internal Schematic Diagram



P-Channel MOSFET

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-38	V
Gate-Source Voltage		V_{GS}	±25	
Continuous Drain Current		I_D	-14	A
Pulsed Drain Current [1)]		I_{DM}	-50	
Maximum Power Dissipation	TA = 25°C	P_D	3.1	W
	TA = 75°C		2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2)]		$R_{\theta JA}$	62.5	°C/W

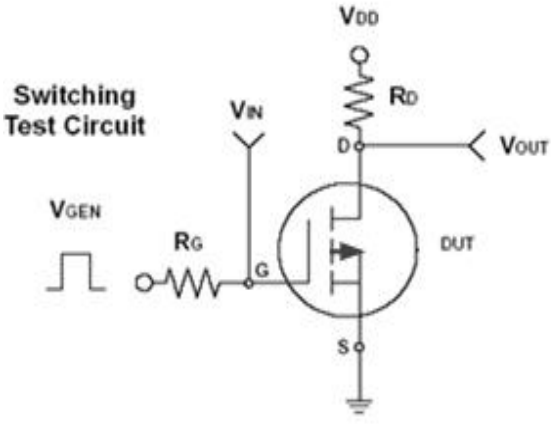
Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature
2. 1-in^2 2oz Cu PCB board

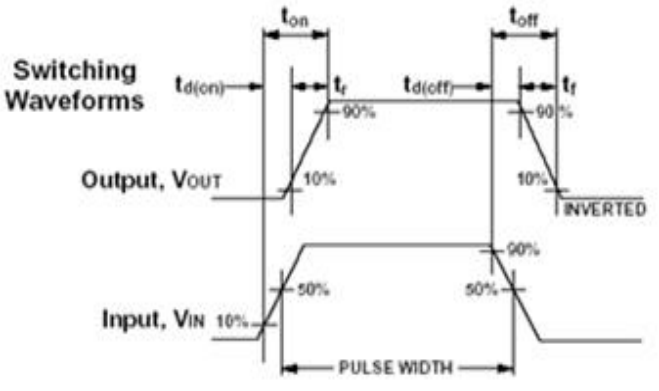
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250uA	-38			V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -14A		11.0	15.0	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = -250uA	-1	-1.8	-3	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -38V, V_{GS} = 0V			-1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ± 25V, V_{DS} = 0V			± 100	nA
Dynamic[3)]						
Total Gate Charge	Q_g	V_{DS} = -20V, I_D = -14A V_{GS} = -10V		62.04		nC
Gate-Source Charge	Q_{gs}			11.24		
Gate-Drain Charge	Q_{gd}			12.40		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -20V, RL= 1.35Ω I_D = -1A, V_{GEN} = -10V R_G = 3Ω		21.08		ns
Turn-On Rise Time	t_r			7.32		
Turn-Off Delay Time	$t_{d(off)}$			84.76		
Turn-Off Fall Time	t_f			17.84		
Input Capacitance	C_{iss}	V_{DS} = -20V, V_{GS} = 0V f = 1.0 MHz		3322.07		pF
Output Capacitance	C_{oss}			332.09		
Reverse Transfer Capacitance	C_{rss}			243.92		
Source-Drain Diode						
Max. Diode Forward Current	I_S				4.2	A
Diode Forward Voltage	V_{SD}	I_S = -1A, V_{GS} = 0V			1	V

Note: Pulse test: pulse width <= 300us, duty cycle<= 2%

3. Guaranteed by design; not subject to production testing





Notice

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2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.