## M-MOS Semiconductor Hong Kong Limited

# 20V P-Channel Enhancement-Mode MOSFET

**$V_{DS}$= -20V**

**$R_{DS(ON)}$, $V_{gs}$@-4.5V, $I_{ds}$@-2.8A = 90mΩ**

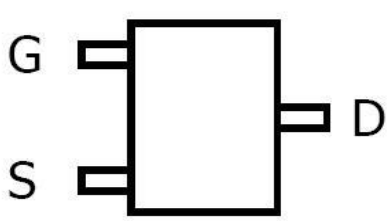
**$R_{DS(ON)}$, $V_{gs}$@-2.5V, $I_{ds}$@-2.0A = 105mΩ**

**$R_{DS(ON)}$, $V_{gs}$@-1.8V, $I_{ds}$@-2.0A = 150mΩ**

## Features

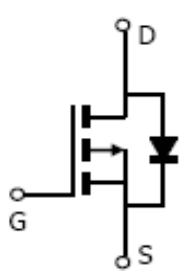
Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance

**SOT- 23**




**Top View**

**Internal Schematic Diagram**




**P-Channel MOSFET**

**Maximum Ratings and Thermal Characteristics** ($T_A$ = 25°C unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 12 | |
| Continuous Drain Current [1)] | | $I_D$ | -2.8 | A |
| Pulsed Drain Current [2)] | | $I_{DM}$ | -8 | |
| Maximum Power Dissipation | TA = 25°C | $P_D$ | 1.25 | W |
| | TA = 75°C | | 0.8 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to 150 | °C |
| Junction-to-Ambient Thermal Resistance (PCB mounted) [3)] | | $R_{\theta JA}$ | 140 | °C/W |

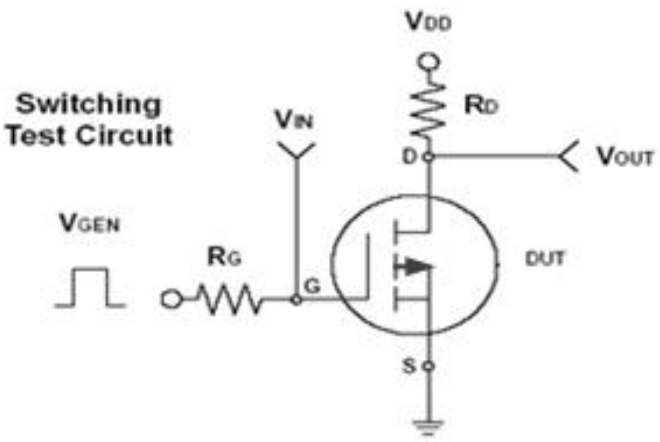
**Note:** 1. Fused current that based on wire numbers and diameter
2. Repetitive Rating: Pulse width limited by the maximum junction temperature
3. 1-in$^2$ 2oz Cu PCB board

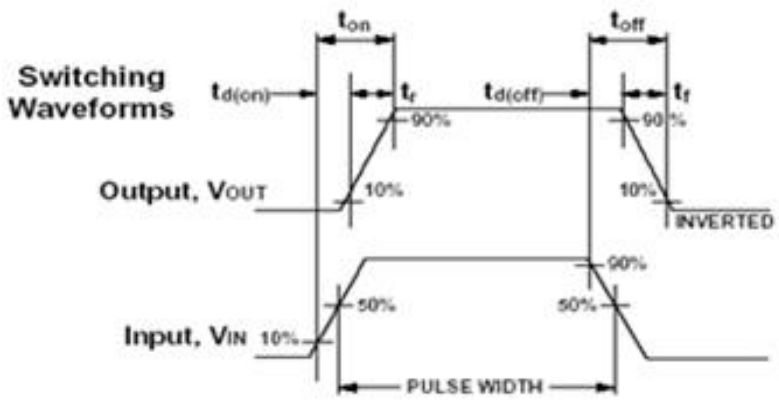
## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250uA | -20 | | | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -4.5V, $I_D$ = -2.8A | | 76 | 90 | mΩ |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -2.5V, $I_D$ = -2.0A | | 91 | 105 | mΩ |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -1.8V, $I_D$ = -2.0A | | 115 | 150 | mΩ |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ =$V_{GS}$, $I_D$ = 250uA | -0.4 | -0.6 | -0.9 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -20V, $V_{GS}$ = 0V | | | -1 | uA |
| Gate Body Leakage | $I_{GSS}$ | $V_{GS}$ = ±12V, $V_{DS}$ = 0V | | | ±100 | nA |
| **Dynamic**[3)] | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = -6V, $I_D$ = -2.8A<br>$V_{GS}$ = -4.5V | | 5.76 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 1.97 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 0.997 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -6V, RL=6Ω<br>$I_D$ = -1A, $V_{GEN}$ = -4.5V<br>$R_G$ = 6Ω | | 7.24 | | ns |
| Turn-On Rise Time | $t_r$ | | | 11.3 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 87.6 | | |
| Turn-Off Fall Time | $t_f$ | | | 41.8 | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = -6V, $V_{GS}$ = 0V<br>f = 1.0 MHz | | 506 | | pF |
| Output Capacitance | $C_{oss}$ | | | 54.8 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 47.3 | | |
| **Source-Drain Diode** | | | | | | |
| Max. Diode Forward Current | $I_S$ | | | | -1.6 | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = -1.6A, $V_{GS}$ = 0V | | 0.821 | | V |

**Note**: Pulse test: pulse width <= 300us, duty cycle<= 2%

3. Guaranteed by design; not subject to production testing



## Typical Characteristics Curves ( Ta=25°C, unless otherwise note )

Fig.1 Output Characteristic

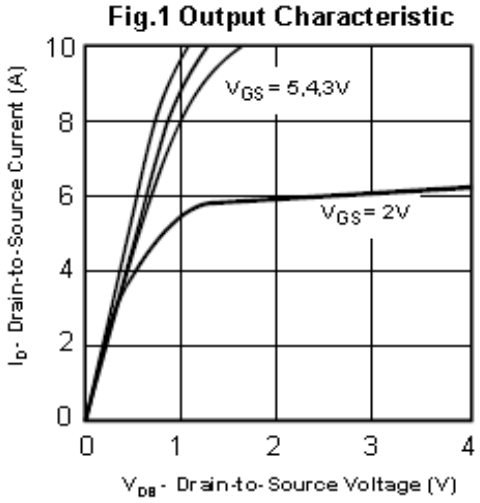



Fig.2 Transfer Characteristics

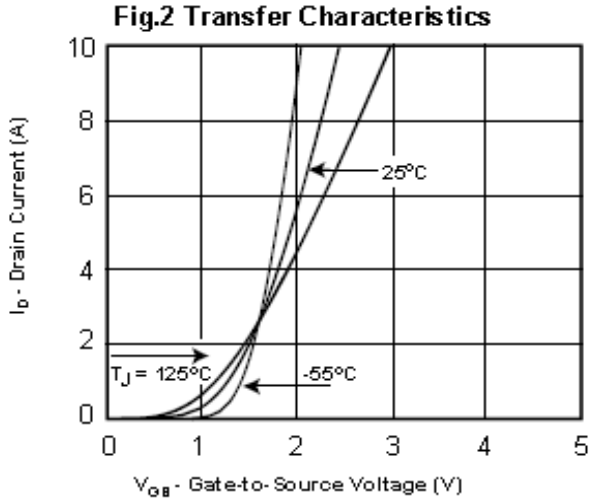



Fig.3 On-Resistance Variation with Temperature

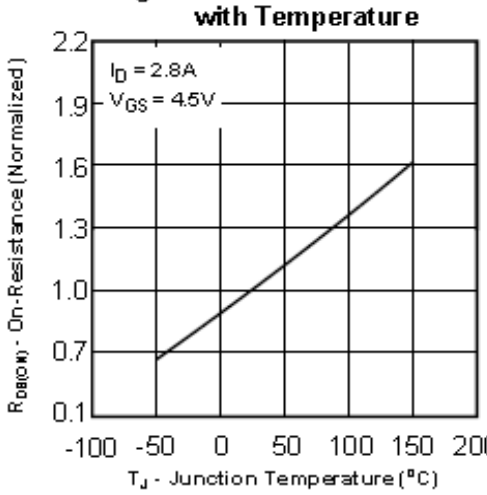



Fig.4 Body Diode Forward Voltage Variation with Source Current

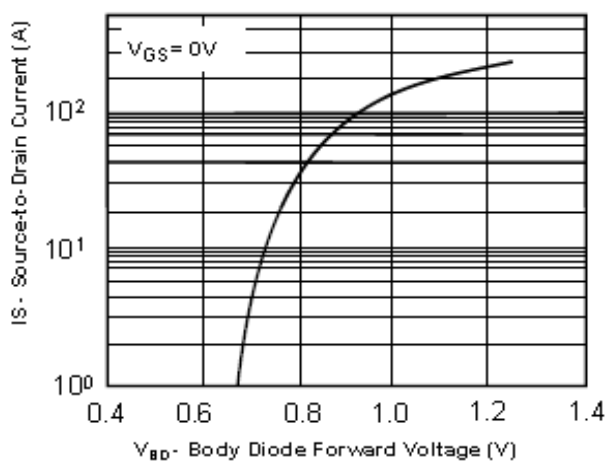



Fig.5 Gate Threshold Variation with Temperature

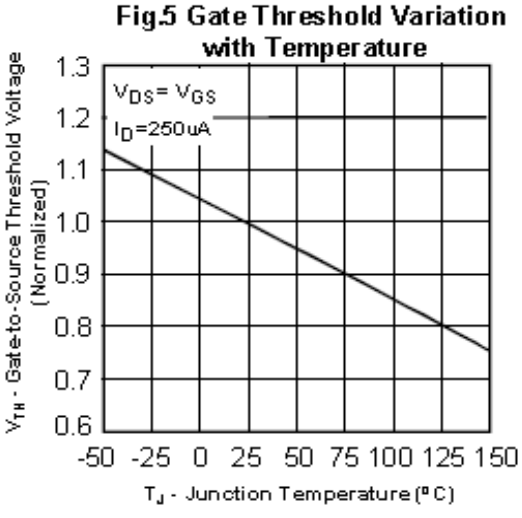
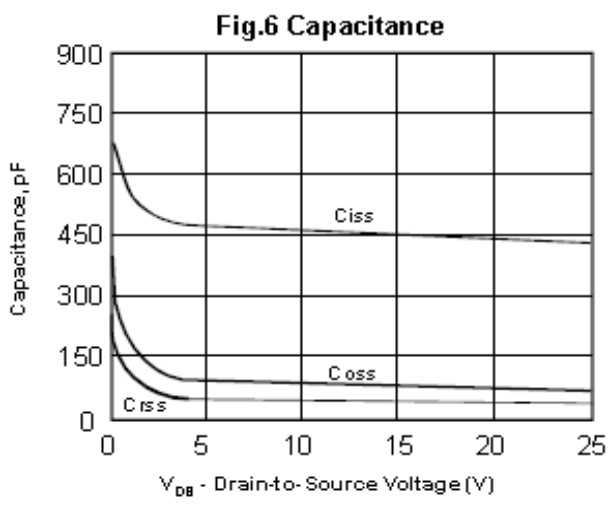



Fig.6 Capacitance



## Typical Characteristics Curves ( Ta=25°C, unless otherwise note )

Fig. 7 Gate Charge Waveform

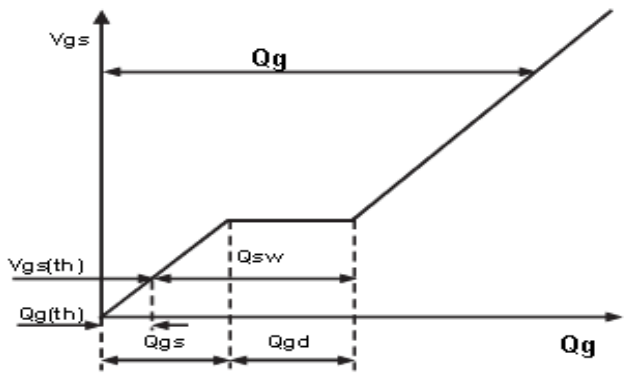



Fig. 8 Gate Charge

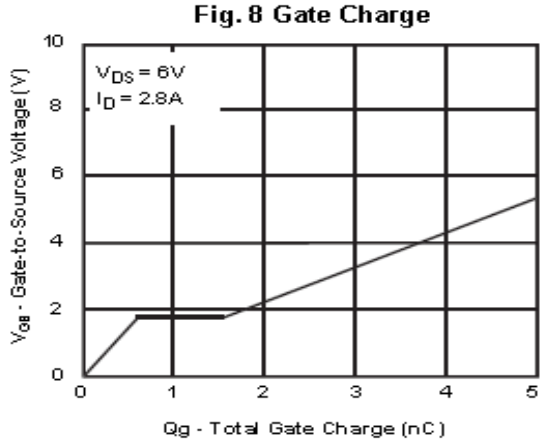



Fig. 9 Maximum Safe Operating Area

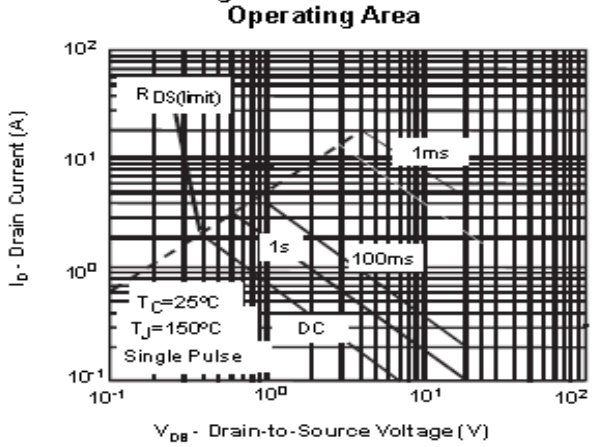
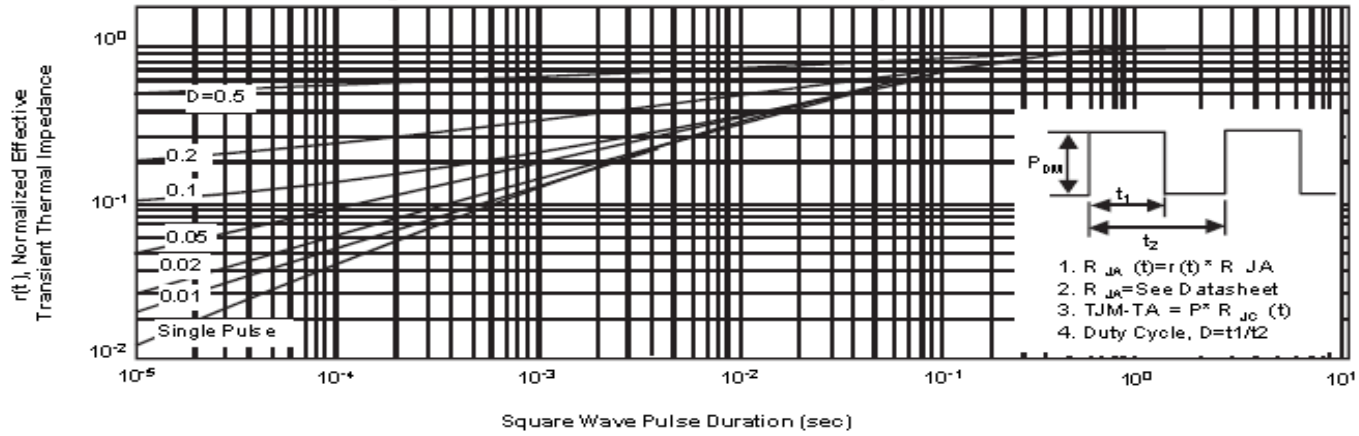



Fig. 10 Normalized Thermal Transient Impedance Curve



# Notice

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**2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**